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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of : Yoshihiro SOTOME
Serial No. : 10/038,680
Filed : January 8, 2002
For : Method of Manufacturing a Semiconductor Device and the Semiconductor Device Manufactured by the Method

DECLARATION

I, Tetsuya KIMURA, declare that I am acquainted with both the Japanese and English languages, that the English translation attached hereto is a true and accurate translation of Japanese Patent Application No. 2001-012035.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Signed at Osaka, Japan on this 30th day of June, 2003

T. Kimura

Tetsuya KIMURA

PATENT OFFICE
JAPANESE GOVERNMENT

This is to certify that the annexed is a true copy of the following application as filed with this office.

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Application Number: Patent Application No. 2001-012035

Applicant(s): SHARP KABUSHIKI KAISHA

Date: November 16, 2001

Commissioner,
Patent Office **K o h z o O I K A W A**

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[Tile of the Invention] Method of Manufacturing a Semiconductor Device and the Semiconductor Device Manufactured by the Method
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[Name of Item] Specification 1
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[Name of Item] Abstract of the Disclosure 1
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【NAME OF THE DOCUMENT】 SPECIFICATION

【TITLE OF THE INVENTION】 METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE AND THE SEMICONDUCTOR DEVICE MANUFACTURED BY THE METHOD

【CLAIMS】

【Claim 1】 A method of manufacturing a semiconductor device characterized by comprising:

the step of forming a first metal film having a reducing property on a semiconductor substrate;

the step of reducing a native oxide film naturally formed on the semiconductor substrate with the first metal film by carrying out a thermal treatment;

the step of forming a silicide film in which the semiconductor substrate is allowed to react with the first metal film on the semiconductor substrate by diffusion limited;

the step of removing an unreacted first metal film selectively;

the step of forming a second metal film on the semiconductor substrate; and

the step of forming a silicide film in which the semiconductor substrate is allowed to react with the second metal film on a surface layer of the semiconductor substrate by carrying out a thermal treatment.

【Claim 2】 A method of manufacturing a semiconductor device according to claim 1, wherein the first metal film is a titanium film.

【Claim 3】 A method of manufacturing a semiconductor device

according to claim 1 or 2, wherein the second metal film is a cobalt film.

【Claim 4】 A method of manufacturing a semiconductor device according to claim 2, wherein by carrying out a thermal treatment at a temperature of 500°C or less, a silicide film in which the semiconductor substrate is allowed to react with the titanium film is formed.

【Claim 5】 A method of manufacturing a semiconductor device according to claim 2 or 4, wherein by carrying out the thermal treatment at the temperature of 500°C or less, the silicide film in which the semiconductor substrate is allowed to react with the titanium film is formed to have a thickness of 1 to 10 nm.

【Claim 6】 A method of manufacturing a semiconductor device according to claim 3, wherein the cobalt film is formed to have a thickness of 1 to 10 nm.

【Claim 7】 A method of manufacturing a semiconductor device according to any of claims 1-6, further comprising the step of forming a protection film on the second metal film for protecting natural oxidization of the second metal film between the step of forming the second metal film and the step of forming a silicide film in which the semiconductor substrate is allowed to react with the second metal film.

【Claim 8】 A method of manufacturing a semiconductor device according to claim 7, wherein the protection film is a titanium nitride film.

【Claim 9】 A method of manufacturing a semiconductor device

according to any of claims 1-8, further comprising the step of oxidizing the semiconductor substrate in a mixed solution of hydrochloric acid, hydrogen peroxide solution and water before the step of forming the first metal film.

【Claim 10】 A method of manufacturing a semiconductor device according to any of claims1-9, wherein the thermal treatment for reducing the natural oxide film is carried out at a substrate temperature at the formation of the first metal film.

【Claim 11】 A semiconductor device manufactured by the method of any of claims 1-10.

【DETAILED DESCRIPTION OF THE INVENTION】

【0001】

【Field of the Invention】

The present invention relates to a method of manufacturing a semiconductor device including a silicide film on a surface of a semiconductor substrate and the semiconductor device manufactured by the method.

【0002】

【Related Art】

In a recent semiconductor device, the performance of the device and the degree of integration are remarkably improved by the advance in minuteness of an element. Especially, in a high speed device to which a minute design rule of 0.35 μm or less is applied, it is necessary to lower parasitic resistance of a diffusion layer as a source/drain region of a MOSFET (Metal Oxide Semiconductor Field

Effect Transistor). Therefore, a SALICIDE (Self Aligned Silicide) is performed to lower the resistance by silicidizing the diffusion layer. The SALICIDE is a technique in which in general, a surface layer of a diffusion layer formed in a silicon substrate and a gate electrode and a field oxide film (element isolation film) are silicidized (converted into, for example, a compound comprising metal such as titanium and silicon) in a self aligned manner, so that the contact resistance between a wiring layer formed on an interlayer insulating film and the diffusion layer are lowered.

【0003】

When a scale-down of a gate is advanced and a gate length becomes short by the improvement in minuteness of an element, a junction depth of the diffusion layer (the depth from the surface of the substrate to the junction of the diffusion layer and the substrate) is relatively increased and a junction of a salicide and the diffusion layer comes close to the junction of the diffusion layer and the substrate. As a result, a leak current in a lateral direction (between source and drain) is increased by a short channel effect, which causes deterioration of element characteristics. Accordingly, in the case where the gate length is made short, it is necessary to make the junction depth of the diffusion layer shallow (shallow junction). Under such circumstances, when the diffusion layer is silicidized, it is necessary to form a silicide layer to be as thin as possible. That is, if the silicide layer is not made sufficiently thin relatively to the junction depth, the silicide layer itself becomes a factor to cause a leak current

in the vertical direction by, for example, diffusion of metal atoms at the time of the reaction of silicidation. However, in the conventional minute design rule of 0.35 μm or 0.25 μm, in the case where a thin silicide layer made of a titanium film is formed, a thin line effect (as line width becomes thin, sheet resistance becomes large) becomes remarkable, and the effect of using the SALICIDE technique disappears.

【0004】

To this problem, in the minute design rule of 0.18 μm or less, a technique using cobalt (Co) silicide having no thin line effect has been reviewed. However, in the case where cobalt is used as a material of the silicide, differently from titanium, since cobalt does not have a reducing property to a native oxide film of the surface of a silicon substrate, there is a problem that a portion where the native oxide film exists is not silicidized, which results in the generation of a patchy reaction of the silicidation and the formation failure of a silicide.

【0005】

To this problem, Japanese Unexamined Patent Publication No. Hei 10(1998)-98012 proposes a method in which a titanium film is formed under a cobalt film. Hereinafter, this method will be described with reference to FIG. 3.

【0006】

First, as shown in FIG. 3(a), a field insulating film 112 for element isolation is selectively formed on a silicon substrate 111 by a normal LOCOS (Local Oxidation of Silicon) process for defining a

MOSFET formation region. A gate electrode 114 made of polycrystalline silicon, etc. is formed in the MOSFET formation region through a gate insulating film 113. Subsequently, a low concentration impurity diffusion layer is formed by ion implanting an impurity into an active region (a region of a surface layer of the silicon substrate 111 which becomes source and drain regions) in order to form an LDD (Lightly Doped Drain) structure, and then a side wall 115 necessary for the formation of the LDD structure is formed on a side surface of the gate electrode 114, and further, an impurity is selectively ion-implanted into the above low concentration impurity diffusion layer to form a source region 116 and a drain region 117 as a high concentration impurity diffusion layer. In this time, native oxide films (SiO_2) 118 are already formed on the surfaces of the source region 116, the drain region 117 and the gate electrode 114. Next, before the formation of a silicide, the substrate is washed to remove the native oxide films 118 formed on the surfaces of the source region 116, the drain region 117, and the gate electrode 114. Incidentally, although the native oxide films 118 become thin by this washing, they are not actually completely removed and remain, or there is also a case where a native oxide film is again formed after the washing. As shown in FIG. 3(b), a thin titanium film 120 is formed on the whole surface of the silicon substrate in order to reduce the native oxide film, and subsequently, a cobalt film 121 for formation of silicide is formed. Next, as shown in FIG. 3(c), that is, a RTA (Rapid Thermal Annealing) treatment is carried out, so that silicon of the gate electrode 114, the

source region 116 and the drain region 117 is made to react with the cobalt film 121, so that silicide films 122 are formed. Next, as shown in FIG. 3(d), the unreacted titanium film 120 and the unreacted cobalt film 121 on the field insulating film 112 and the side wall 115 are removed by selective etching, a second RTA treatment is further carried out in order to lower the resistance of the silicide films 122. By this, a MOSFET having SALICIDE structure is formed, in which the silicide films 122 are formed in a self aligned manner only on the gate electrode 114, the source region 116 and the drain region 117.

【0007】

【Problem that the Invention is to solve】

However, in the above method, it is necessary to control the under titanium film to be thin so that the main ingredient in the silicide film becomes cobalt in order to obtain the thin and uniform silicide film having no thin line effect, but the method is not suitable for further minuteness and thinning of a semiconductor divice.

【0008】

Generally, a cobalt silicide is formed to have a thickness about 3.5 times as thick as a cobalt film, and a titanium silicide is formed to have a thickness about 2.4 times as thick as a titanium film, and in order to suppress the thin line effect, it is necessary that the thickness of the titanium silicide film is controlled to be about 20 percent of the thickness of the cobalt silicide film. Accordingly, for example, if the thickness of the cobalt film is 5 nm, the thickness of the cobalt silicide becomes about 17.5 nm, and in this case, in order to make the

thickness of the titanium silicide about 20 percent (about 3.5 nm) of that of the cobalt silicide, the thickness of the titanium film is made as thin as about 1.4 nm. There is a problem that it is very difficult to control the titanium film to become such a thin thickness, thereby to form a thin titanium. Besides, since the titanium film is apt to react with oxygen, the thinner the titanium film is made, the greater the influence of an atmosphere becomes, and there is another problem that the reducing property to the native oxide film can not be expected by the influence of oxidation from the surface side of the substrate.

【0009】

【Means of solving the problem】

As a result of an intensive study in view of the above problems, solving of the above problems is found out and the present invention is achieved by forming a first metal film having a reducing property on a semiconductor substrate, reducing a native oxide film, forming a silicide film made of the first metal film by diffusion limited, removing an unreacted first metal film, thereby forming a silicide film made of a second metal film.

【0010】

According to the present invention, there is provided a method of manufacturing a semiconductor device characterized by comprising: the step of forming the first metal film having the reducing property on the semiconductor substrate; the step of reducing a native oxide film naturally formed on the semiconductor substrate by carrying out a thermal treatment; the step of forming a silicide film in which the

semiconductor substrate is allowed to react with the first metal film on the semiconductor substrate by the diffusion limited; the step of removing an unreacted first metal film selectively; the step of forming a second metal film on the semiconductor substrate; and the step of forming a silicide film in which the semiconductor substrate is allowed to react with the second metal film on a surface layer of the semiconductor substrate by carrying out the thermal treatment.

【0011】

Further, according to the present invention, there is provided a semiconductor device manufactured by the above described method.

【0012】

【Embodiment】

The present invention will be described in detail with reference to the drawings.

【0013】

FIG. 1 is a process sectional view showing an embodiment of the present invention.

【0014】

First, as shown in FIG. 1(a), a field insulating film 12 for element isolation is selectively formed by a normal LOCOS process on a p-type silicon substrate 11 as a semiconductor substrate for defining a MOSFET formation region.

【0015】

Materials for constituting the semiconductor substrate are selected appropriately from known materials in order to adapt to the

semiconductor device to be manufactured. For example, elementary semiconductors such as silicon, Ge, Sn, Se and the like, compound semiconductors such as GaAs, GaP, AlGaAs and the like, and oxide semiconductors such as SnO_2, ZnO and the like are cited. Among them, the silicon is preferable on the point that the effect of the present invention is remarkable.

【0016】

Next, the surface of the silicon substrate 11 in the MOSFET formation region is oxidized by a thermal oxidation or the like so that a gate insulating film 13 is formed to have a thickness of about 3 nm. Then, a gate electrode layer made of a polycrystalline silicon (polysilicon) film is formed to have a thickness of about 200 nm by a low pressure CVD method or the like. Incidentally, the gate electrode layer may be made to have a polycide structure in which a WSi_x (tungsten silicide) layer is stacked on the polycrystalline silicon. Next, a photoresist film (not shown) is formed on the gate electrode layer, and pattered by a photolithography technique. The gate electrode layer is selectively etched and processed to form a gate electrode 14 using the patterned photoresist film as an etching mask. In order to form an LDD structure, an n-type impurity is ion-implanted into an active region (region of a surface layer of the silicon substrate 11 which becomes source and drain regions) to form a low concentration n-type impurity diffusion layer. An insulating film is formed and then the insulating film is subjected to anisotropic etching to form a side wall 15, which is required for the formation of the LDD structure, at a side

surface of the gate electrode 14. Further, an n^+type impurity is selectively ion-implanted into the n-type impurity diffusion layer to form a source region 16 and a drain region 17 as a high concentration n^+type impurity diffusion layer. At this time, native oxide films (SiO_2) 18 are already formed on the surfaces of the source region 16, the drain region 17 and the gate electrode 14. Subsequently, the silicon substrate 11 is washed by, for example, a dilute hydrofluoric acid of a concentration of 1% to remove the native oxide films 18. However, although the native oxide films become thin by this washing, they are not actually completely removed, or a native oxide film is again formed after the washing.

【0017】

Incidentally, after the native oxide films are removed, if an oxide film is uniformly formed on the substrate by dipping the whole silicon substrate in a mixed solution of, for example, ammonium hydroxide, hydrogen peroxide solution and water or a mixed solution of hydrochloric acid, hydrogen peroxide solution and water, it becomes possible to suppress formation of an irregular native oxide film, and a silicide film can be formed more uniformly, so that this is preferable. In the above mixed solutions, it is preferable to use the mixed solution of hydrochloric acid, hydrogen peroxide solution and water in that the silicide film can be more uniformly formed.

【0018】

It is preferable that the ammonium hydroxide, hydrogen peroxide solution and water are used in a proportion of 1:1:5, but the

proportion of water can be adjusted within a range of 4 to 50.

【0019】

It is preferable that the hydrochloric acid, hydrogen peroxide solution and water are used in a proportion of 1:1:5, but the proportion of water can be adjusted within a range of 4 to 50.

【0020】

Next, as shown in FIG. 1(b), a titanium (Ti) film 20 as a first metal film having a reducing property is formed to have a thickness of about 20 nm on the whole surface of the silicon substrate 11.

【0021】

The first metal film is formed by a well-known method, for example, sputtering. In this embodiment, although sputtering is carried out at a substrate temperature of about 350°C, the temperature is not limited to this, but sputtering can be normally carried out at about 300 to 450°C.

【0022】

The first metal film is not particularly limited as long as it has a reducing property to a native oxide film, but it is preferable to use a titanium film in that the effect of the present invention can be excellently obtained. Besides, the thickness of the first metal film is not particularly limited as long as the native oxide film can be sufficiently reduced and an obtained silicide film does not have a thickness such that the thin line effect is caused, but it is preferable that the thickness is about 10 to 40 nm.

【0023】

Next, a thermal treatment is carried out so that the native oxide films 18 are reduced by the titanium film 20, and further, silicon in the silicon substrate 11 is made to react with titanium in the titanium film 20 by diffusion limited to obtain a titanium silicide film 25 of about 3 nm-thickness.

【0024】

Incidentally, the temperature of the thermal treatment is usually a substrate temperature at the formation of the titanium film or the temperature at the formation of the titanium silicide film. The temperature of the thermal treatment is not particularly limited, but preferably about 500℃ or less, more preferably about 200 to 400℃. The thickness of the titanium silicide film 25 is preferably 1 to 10 nm, and more preferably 2 to 5 nm.

【0025】

The titanium film of the unreacted first electric layer is selectively removed.

【0026】

The removal of the unreacted first electric layer can be carried out by a well-known method, for example, wet etching or the like. In this embodiment, the wet etching is carried out by using, for example, a mixed solution of sulfuric acid and hydrogen peroxide solution of 4:1.

【0027】

Next, as shown in FIG. 1(c), a cobalt film 21 as a second metal film is formed to have a thickness of about 5 nm on the whole surface of the silicon substrate 11.

【0028】

The second metal film is formed by, similarly to the first metal film, a well-known method, for example, sputtering or the like.

【0029】

For example, a cobalt film, a nickel film or the like is cited as the second metal film, however, it is preferable to use the cobalt film in that there is no the thin line effect. The thickness of the cobalt film is preferably about 1 to 10 nm, more preferably about 3 to 8 nm.

【0030】

Next, as shown in FIG. 1(d), by carrying out a thermal treatment, silicon in the gate electrode 14, the source region 16 and the drain region 17 is made to react with the cobalt film 21 and cobalt silicide films 22 are formed to have a thickness of about 17.5 nm on the surface layer of the silicon substrate.

【0031】

Well-known methods may be used for a method of carrying out the thermal treatment in accordance with the kind of material of the second metal film to be used. The method can be carried out by, for example, a RTA treatment. Specifically, in this embodiment, the RTA treatment is carried out under the conditions of a nitrogen atmosphere, atmospheric pressure, 550°C and 60 seconds, but the conditions is not particularly limited.

【0032】

It is preferable that the thickness of the cobalt silicide film is about 3.5 to 35 nm. Incidentally, since it is hard to make the silicon

oxide film react with the cobalt film, the cobalt silicide film is not formed on the field insulating film 12 and the side wall 15, and the unreacted cobalt film 21 remains. Next, although not shown, the unreacted cobalt film 21 on the field insulating film 12 and the side wall 15 is selectively wet etched and removed by, for example, a mixed solution of sulfuric acid and hydrogen peroxide solution of 4:1. Next, for the purpose of lowering the resistance of the cobalt silicide film 22, a second RTA treatment can be carried out, for example under the conditions of a nitrogen atmosphere, atmospheric pressure, 700°C and 30 seconds. In this way, the cobalt silicide films 22 are formed in the self aligned manner only on the gate electrode 14, the source region 16 and the drain region 17, thereby to form a salicide structure. Thereafter, although not shown, an interlayer insulating film, a wiring layer, a contact between the substrate and a wiring line and the like are formed, and then a protection film is formed, thus an n-channel type MOSFET is manufactured.

【0033】

Next, another embodiment of the present invention will be described with reference to the drawings.

【0034】

FIG. 2 is a process sectional view showing another embodiment of the present invention.

【0035】

In this embodiment, since steps (FIGS. 2(a), 2(b) and 2(c)) up to a step in which a titanium film 20 is formed are carried out in the

same way as the former embodiment (FIGS. 1(a), 1(b) and 1(c)), the description is omitted.

【0036】

In another embodiment, as shown in FIG. 2(c), after a cobalt film 21 as a second metal film is formed to have a thickness of about 5 nm on the whole surface of a silicon substrate 11, a titanium nitride film (TiN film) 24 as a protection film is further formed thereon to have a thickness of about 30 nm.

【0037】

By forming the protection film, it is possible to prevent the second metal film from being once exposed to the air and oxidized during transport to a RTA apparatus in a subsequent RTA treatment step, and it is also possible to effectively prevent oxygen from being taken into the silicide film. Thus, it is further effective in lowering of the resistance of the silicide film.

【0038】

The protection film is preferably etched similarly to the unreacted second metal film at the selective etching of the later step, for example, a nitride film may be mentioned. Also, it is preferable that the thickness of the protection film is about 20 to 40 nm.

【0039】

Next, by carrying out a thermal treatment, the silicon substrate 11 is made to react with the cobalt film 21, cobalt silicide films 22 are formed, and then the unreacted cobalt film and titanium nitride film are removed by wet etching of, for example, a mixed solution of sulfuric

acid and hydrogen peroxide solution of 4:1.

【0040】

Other steps and effects are the same as the aforementioned embodiment.

【0041】

As described above, although the two embodiments are exemplified to describe the manufacturing method of the present invention, the present invention is not limited to these embodiments, but various modifications can be made within the scope of the equivalent. Accordingly, in the above-mentioned respective embodiments, although the description has been given of the manufacturing method of the n-channel type MOSFET which is constructed by silicidizing the source and drain regions, the method of the present invention can also be applied to a manufacturing method of, for example, a p-channel type MOSFET or a CMOS (complementary MOS) FET, and further, can also be applied to a manufacturing method of a device of a MIS (Metal Insulator Semiconductor) type structure.

【0042】

【Effect of the Invention】

As described above, according to the method of manufacturing the semiconductor device of the present invention, the first metal film having the reducing property is preformed and carried out the thermal treatment, so that the under native oxide film is reduced. Thus, it is possible to avoid such disadvantages that the silicide film is not formed

by the existence of the native oxide film or the thickness of the silicide film becomes irregular.

【0043】

Besides, since the silicide film made of the semiconductor substrate and the first metal film can be formed to be thin by diffusion limited, it is possible to suppress the influence on properties of the silicide film made of the semiconductor substrate and the second metal film to be low.

【0044】

Further, since silicidation is carried out by forming the second metal film after the unreacted first metal film is removed, the thin line effect caused by the first metal film can also be avoided.

【0045】

Particularly, in the case where the titanium film is used as the first metal film and the cobalt film not having the thin line effect is used as the second metal film, the thickness of the silicide film made of the titanium film is to be 10 nm or less and the thickness of the cobalt film is to be 10nm or less by carrying out the thermal treatment at a temperature of 500℃ or less or the temperature at the formation of the titanium film, and then the native oxide film is reduced with the titanium film. Thus, it is possible to avoid an adverse effect by the native oxide film when the formation of the cobalt silicide. That is, the thickness of the silicide film inside wafers can be made thin and sufficiently uniform. In the finally obtained silicide film, it becomes possible to suppress the titanium silicide component to be low as

compared with the cobalt silicide component. By this, it becomes possible to lower the fluctuation of sheet resistance including a thin line portion, and it also becomes unnecessary to control the thickness of the titanium film to be not larger than the thickness of the cobalt film.

【0046】

Therefore, according to the method of the present invention, in future, in accordance with the development in the shallow junction of a MOSFET in which its source and drain are silicidized, the silicide film containing cobalt silicide as its main ingredient can be formed to be thin and uniform by the simple method, and accordingly, the thin line effect and the junction leak do not occur, and the parasitic resistance of a diffusion region, a gate region and a contact portion can be lowered.

【BRIEF DESCRIPTION OF THE DRAWINGS】

【Fig. 1】

Process sectional views showing a method of manufacturing a semiconductor device according to an embodiment of the present invention.

【Fig. 2】

Process sectional views showing a method of manufacturing a semiconductor device according to another embodiment of the present invention.

【Fig. 3】

Process sectional views showing a method of manufacturing a

conventional semiconductor device.

【EXPLANATION OF THE REFERENCE NUMERALS】

11, 111	silicon substrates
12, 112	field insulating films
13, 113	gate insulating films
14, 114	gate electrodes
15, 115	side walls
16, 116	source regions
17, 117	drain regions
18, 118	native oxide films
20, 120	titanium films (first metal films)
21, 121	cobalt films (second metal films)
22, 122	cobalt silicide films
24	a titanium nitride film (a protection film)
25	titanium silicide

【NAME OF THE DOCUMENT】 ABSTRACT

【ABSTRACT】

【OBJECT】 To provide a method of manufacturing a semiconductor device suitable for the minuteness and thinning of the semiconductor device.

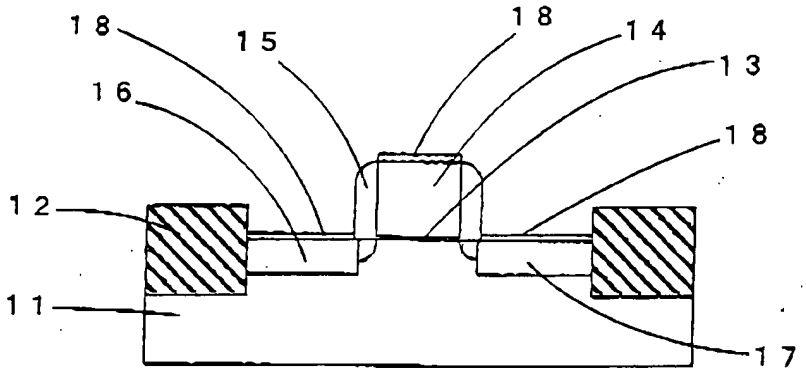
【MEANS OF SOLVING】 The above object is solved by providing a method of manufacturing a semiconductor device characterized by comprising: the step of forming a first metal film having a reducing property on a semiconductor substrate; the step of reducing a native oxide film naturally formed on the semiconductor substrate by the first metal film by carrying out a thermal treatment; the step of forming a silicide film in which the semiconductor substrate is allowed to react with the first metal film on the semiconductor substrate by diffusion limited; the step of removing an unreacted first metal film selectively; the step of forming a second metal film on the semiconductor substrate; and the step of forming a silicide film in which the semiconductor substrate is allowed to react with the second metal film on a surface layer of the semiconductor substrate by carrying out a thermal treatment.

【SELECTED FIGURE】 FIG. 1

【NAME OF THE DOCUMENT】 Drawings

【FIG.1】

(a)



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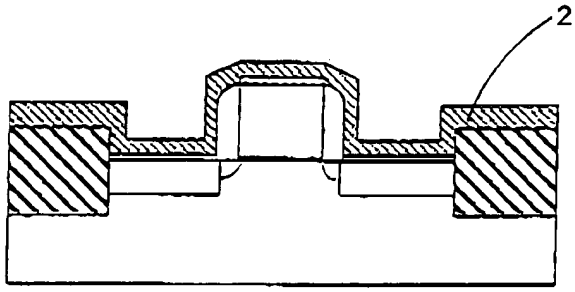

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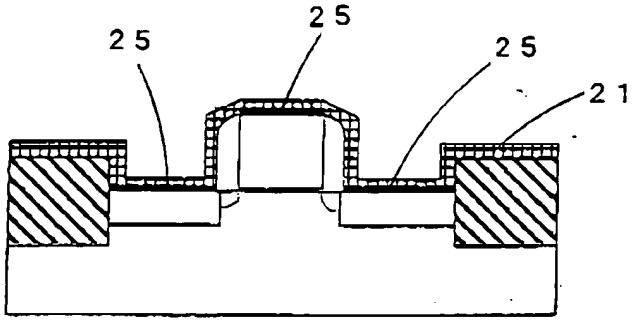
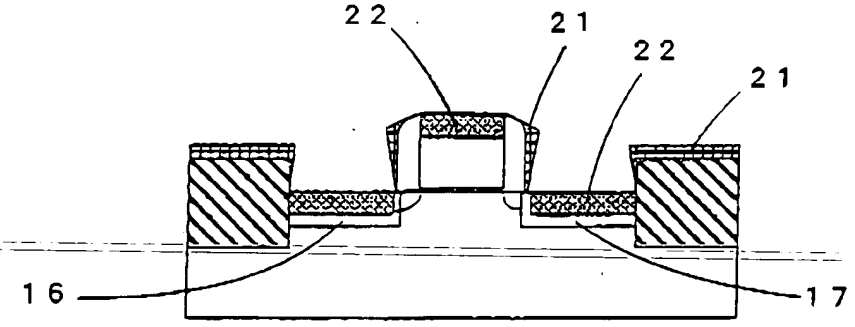
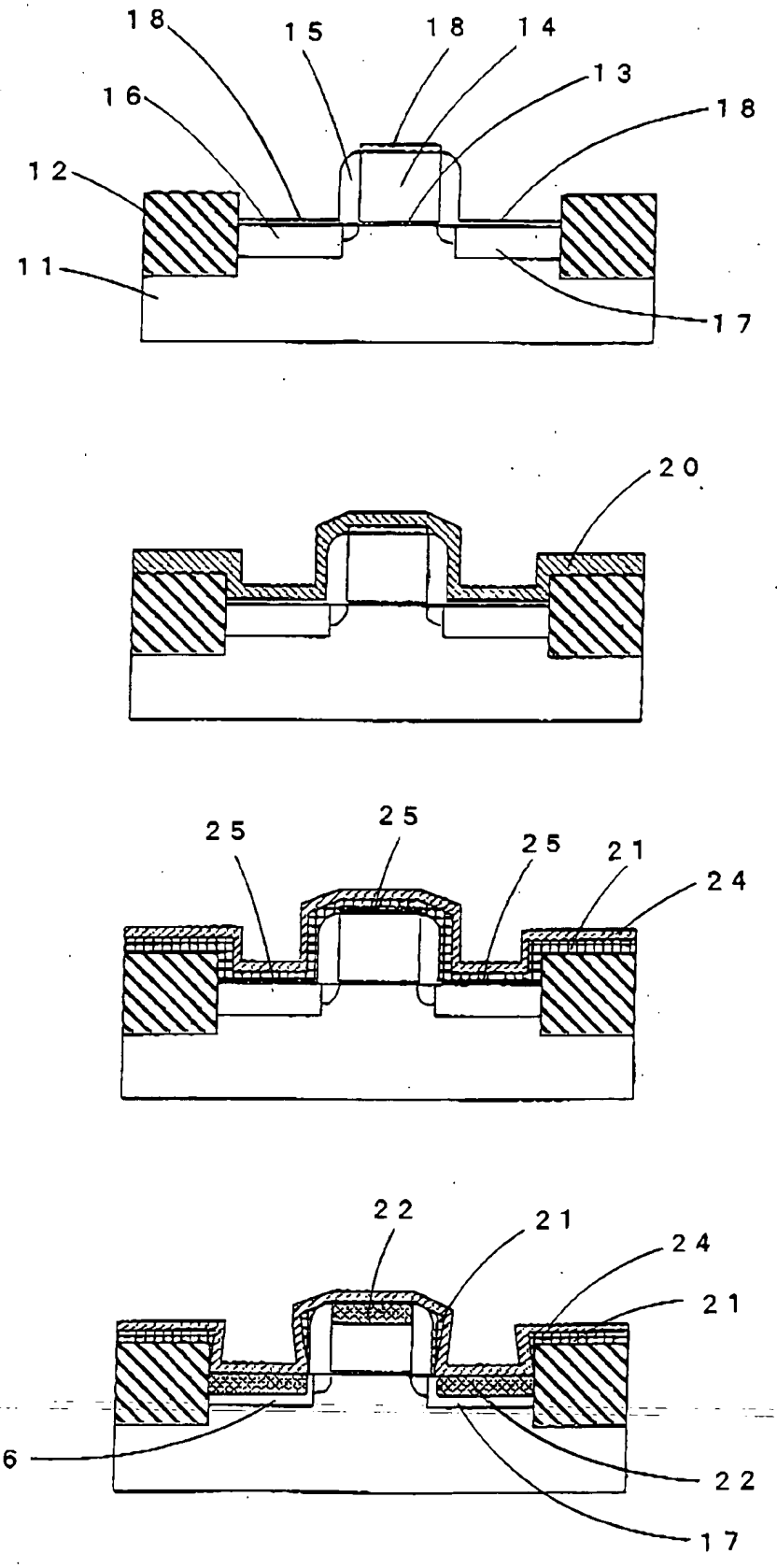


(d)



【FIG.2】


(a)
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(b)
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(c)
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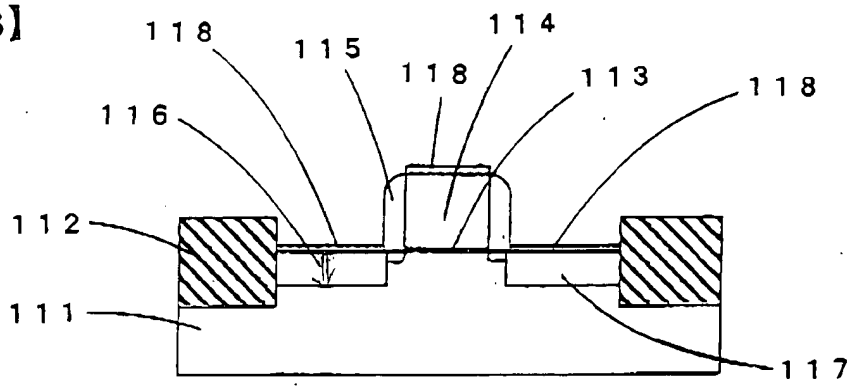
【FIG.3】

(a)


118
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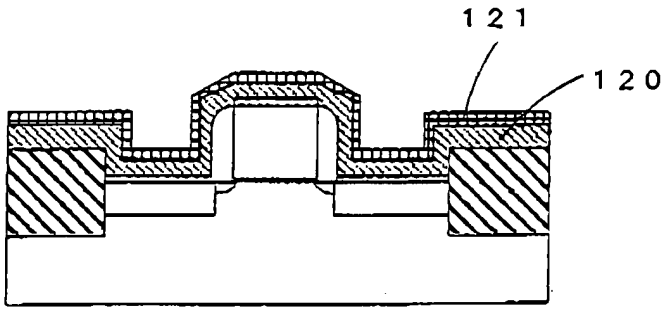
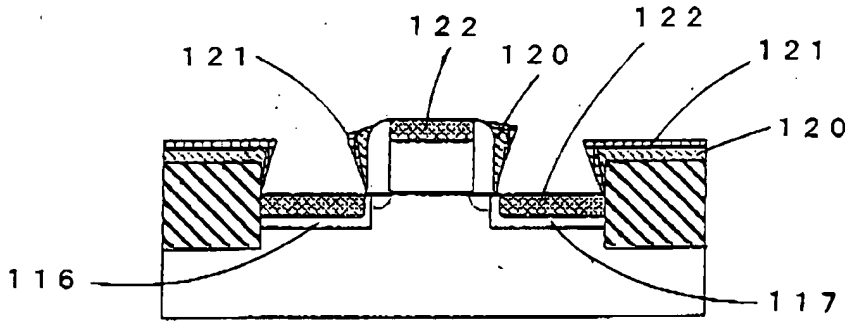
117

(b)


121
120

(c)


122
122
121
120
121
120
116
117

(d)